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PTO/SB/05 (12/97)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	**TI-21556**
First Named Inventor or Application Identifier	**Sami Kiriaki**
Title	**Differential, High Speed, Ecl To Cmos Converter**
Express Mail Label No.	**EL008140088US**

07/27/98 jc595 U.S. PTO

jc560 U.S. PTO 09/123208 07/27/98

APPLICATION ELEMENTS

See MPEP Chapter 600 concerning utility patent application contents

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original, and a duplicate for fee processing)
2. [X] Specification *(preferred arrangement set forth below)* [Total Pages **10**]
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R&D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC d113)* [Total Sheets **2**]
4. Oath or Declaration [Total Pages]
   a. [ ] Newly Executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR §1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identical of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & Documents(s))
9. [ ] 37 CFR §3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] *Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other:

**A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.*

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: /

Prior application information: Examiner ________ ***Group / Art Unit:*** ________

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [X] *Correspondence address below*

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Name (Print/Type)	**Leo N. Heiting**	*Registration No. (Attorney/Agent)*	**26,906**
Signature	Leo N. Heiting	*Date*	7/27/98

FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.
These are the fees effective October 1, 1997
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.

TOTAL AMOUNT OF PAYMENT	($) 790.00

Complete If Known	
Application Number	TBD
Filing Date	July 24, 1998
First Named Inventor	Sami Kiriaki
Examiner Name	TBD
Group / Art Unit	TBD
Attorney Docket No.	TI-21556

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge to the following Deposit Account,

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Deposit Account Name: Texas Instruments

☒ Charge any additional fee required or credit any overpayment

☐ Charge all indicated fees and any additional fee required or credit any overpayment

2. ☐ **Payment Enclosed:**

☐ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	$790
106	330	206	165	Design filing fee	$
107	540	207	270	Plant filing fee	$
108	790	208	395	Reissue filing fee	$
114	150	214	75	Provisional filing fee	$

SUBTOTAL (1) ($)790

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	9	-20** =	0	x	22	=	0
Independent Claims	3	-3** =	0	x	82	=	0
Multiple Dependent						=	0

***or number previously paid, if greater; For Reissue, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent Claims in excess of 3
104	270	204	135	Multiple dependent claims in excess of 3
109	82	209	41	**Reissue independent claims over original patent
110	22	210	11	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)0

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension of time within second month	
117	950	217	475	Extension of time within third month	
118	1,510	218	755	Extension of time within fourth month	
128	2,060	228	1,030	Extension of time within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a pubic use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt.	
581	40	581	40	Recording each patent assignment per property (time number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) ____________

Other fee (specify) ____________

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3)

SUBMITTED BY		Complete (if applicable)	
Typed or Printed Name	Leo N. Heiting	Reg. Number	26,906
Signature	Leo N. Heiting — Date 7/27/98	Deposit Account User ID	

DIFFERENTIAL, HIGH SPEED, ECL TO CMOS CONVERTER

BACKGROUND OF THE INVENTION

Cross-Reference to Related Application

This invention is related to the invention disclosed and claimed in co-pending U.S. Patent Application, filed of even date with the filing date of this Application and bearing Attorney's Docket No. TI-21557, the contents of which are hereby incorporated by reference in this Application. .

Field of the Invention

This invention relates to the interfacing of high speed, low voltage, data streams with CMOS circuits and, more specifically, to converting low voltage, differential, ECL signal levels to higher voltage levels which are compatible with CMOS circuits while maintaining high speed and sufficient drive capability.

Brief Description of the Prior Art

Differential Emitter Coupled Logic (ECL) circuitry is often used in high speed data transmission applications due to its small signal nature and resulting higher speed of operation. The differential aspect of these low level signals provides improved signal-to-noise, due to common mode operation at the receiving end of the transmission. However, it is important that these low level ECL signals be converted to higher levels without a significant degradation in speed and that the output of the converter has sufficient drive capability to make it useful for a particular application.

Existing circuits of this type often make the ECL to CMOS level conversion at the

expense of speed and/or drive capability. Inherently, the lower ECL levels can be switched faster than the larger CMOS levels, but attempts to speed up the conversion process often diminish the output drive capability of the circuit. Representative prior circuits of this general type are shown in U.S. Patent Nos. 5,726,588 to Fiedler, 5,606,268 to Van Brunt and 5,426,381 to Flannagan et al. None of these patents discloses or suggests the novel features of the present invention..

.SUMMARY OF THE INVENTION

This invention addresses the conversion of small ECL level signals to CMOS level (typically 5 volt or greater) signals with the highest possible speed and drive capability. The basic approach in the invention is to keep the circuitry simple with as few parts as possible, since generally, the fewer the number of parts, the faster the circuit will be.

Briefly, a differential pre-amplifier with constant current source is used to dynamically sink and source current in the two legs of the amplifier based on the ECL signal levels at the input of the amplifier. In order to achieve the highest possible speed, the load capacitance at the output of the differential pre-amplifier is kept as small as possible. This is accomplished by designing the first stage inverters or other form of buffers, which are driven by the differential pre-amplifier, with the smallest possible geometries on the integrated circuit;. Drive capability is then provided by means of an additional buffer which may take the form of an inverter. Drive capability for large capacitive loads is then provided by means of additional buffers at the outputs of the circuit.

In the preferred embodiment, a provision for driving higher loading conditions such as may be found in systems applications is included. The achievement of this level of drive capability often involves multiple buffering and complexity in the circuitry which in turn causes a

degradation in speed. To overcome this, a cross-coupled emitter follower is used to address both the speed and drive capability requirements. The normal load resistors in these cross-coupled emitter followers are replaced by N-channel MOSFETs. The emitter followers are designed with higher load capability through the expedient of driving the gates of these MOSFET loads from the complementary cross-coupled signal to help speed up the response of the output signal. If, for example, the output of the emitter follower is to go high, the load MOSFET is assisted in turning off at a faster rate by this cross-coupling. The minimization of the capacitive loading on the differential pre-amplifier and the provision of larger geometry bipolar emitter followers with complementary feedback to provide necessary drive capability for large capacitive loads results in a uniquely fast and powerful converter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates the ECL to CMOS levels involved in the conversion.

FIG. 2 shows a block diagram for the ECL to CMOS converter.

FIG. 3 shows a schematic circuit diagram for the ECL to CMOS converter.

FIG. 4 illustrates the operation for an optional pull-up transistor at the complementary outputs of the circuit to provide rail-to-rail voltage swing.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1 illustrates the ECL to CMOS conversion process. As shown, at the present state of the art, the differential ECL input pulse V_i can have an amplitude as low as 0.3 volts while the resulting complementary CMOS output pulse V_o can be as large as 5 volts or greater. In Figure 1, t_d indicates the delay time between the ECL input and CMOS output pulses while t_r and t_f

represent the rise and fall times of the CMOS output pulse. The goal of the circuit is to keep these parameters as small as possible in order to maintain high speed operation.

Figure 2 is a block diagram of the preferred embodiment of the invention. In this embodiment, the differential pre-amplifier consists of a basic differential amplifier 1 and a constant current source 2. Complementary ECL inputs ECL- and ECL+ are coupled to the inputs of the differential pre-amplifier. The differential outputs of the pre-amplifier drive circuit nodes A and C. A goal of the circuit design is to maintain the capacitance at these two nodes, shown as phantom capacitors 3 and 4 respectively, as low as possible. The outputs of the differential pre-amplifier drive inverters 5 and 6. These inverters are labeled I_x, where x indicates minimum geometries for the design rules being used. Keeping these inverters small tends to lower the capacitance at nodes A and C which in turn enhances the speed of the circuit. While inverters are used in the preferred embodiment, it is equally within the contemplation of the invention that non-inverting buffers can be employed as an alternative. This element, whether inverting or not, may alternatively be referred to as an inverter, buffer, buffer stage o or intermediate buffer. Although the outputs of inverters 5 and 6 switch between CMOS levels V_d and V_s and have a fast response, their drive capability is limited. For purposes of this description, V_d and V_s are assumed to be five volts and ground, although they are not limited to these values.

To provide the desired drive capability, two buffer circuits 7 and 8 are added. Basically, these buffers are emitter followers with cross-coupled load transistors which are driven from the complementary side of the circuit. nodes D and B, to speed up the switching time of the buffers. The outputs of buffers 7 and 8 are capable of driving larger system type capacitive loads,

emulated as phantom capacitors 11 and 12. These are not part of the circuit, but simply represent the larger loading capability at the outputs.

Also shown are optional output pull-up stages 9 and 10 which can be added for those applications requiring that the output swing be between the CMOS rails, Vd and V_s.

Figure 3 shows a detailed schematic for an implementation of the circuit. As discussed earlier, the CMOS levels of V_d and V_s may be +5V and ground. Here the differential pre-amplifier consists of transistors 22 and 23 and resistors 20 and 21 along with a constant current source 24. The small differential ECL level inputs signals, labeled ECL+ and ECL-, at the base of transistors 22 and 23, respectively direct the sourcing and sinking of current in the two legs of the amplifier. The outputs of the differential pre-amplifier drive the minimum capacitance at nodes A and C and are the inputs to inverters on each side of the complementary circuit. These inverters are comprised of transistor pairs 25-26 and 27-28. Each inverter includes a p-channel transistor 25 or 27 and an n-channel transistor 26 or 28. These inverters are designed to have the minimum component dimensions possible for the chosen process design rules being used in the design so as to keep the capacitance at nodes A and C low. The output of these inverters, shown at nodes B and D, are at CMOS levels and complementary to the signals from the differential pre-amplifier, i.e., if the; ECL+ signal goes high, ;the amplifier output at node A tends to go low and the inverter output at node B goes high. These first stage inverters, however, have only limited drive capability due to the size of their components.

To provide the desired drive capability, buffer circuits are added at the outputs of the first inverters at nodes B and D. These buffers consist of two bipolar transistors 29 and 31 and two n-

channel transistors 30 and 32. These circuits are much like normal emitter followers with the exception that the gates of the two n-channel load transistors are cross-coupled to the corresponding complementary signals from nodes D and B, respectively. This feature is used to speed up the response time of the ECL to CMOS converter. For example, if the output of the buffer 29-30 is going high, the input to the gate of load transistor 30, driven from the output of inverter 27-28 at node D, is going low to help turn off transistor 30 faster and speed up operation of the circuit. As a result, this ECL to CMOS converter can drive the large system level loads, indicated as phantom capacitors 35 and 36 and still operate at relatively high speeds. Since the emitter followers are non-inverting, the complementary output signals will have the same polarity as the outputs of the first inverters at nodes B and D.

Optional p-channel pull-up transistors 33 and 34 can be added for applications which require full complementary CMOS levels which swing between V_d and V_s. As shown in Figure 3, these optional transistors are driven at their gates by the same cross-coupled complementary signals from nodes A and B as used to drive transistors 30 and 32. The operation of these pull-up transistors is illustrated in Figure 4.

Without the pull-up transistors, when the output of the converter goes high, the signal level will quickly rise and settle at a voltage equal to V_d - $V_{be.}$ where V_{be} is the base-to- emitter voltage of bipolar transistors 29 and 31. This is illustrated in Figure 4 which shows the rise in output voltage when the ECL input voltage changes state. In the ideal waveform shown, the output voltage rises instantaneously to the supply voltage, $V_{d,}$ and remains there until the input again changes state. In the actual circuit, however, the rise in output voltage is rapid but less than

instantaneous, and settles at the value $V_d - V_{be}$ as shown.in Figure 4.

When pull-up transistors 33 and 34 are added to the circuit, however, the output signals can pull all the way up to V_d, although at a slightly slower rate as illustrated in Figure 4. For example with reference to Figure 3, if the output of the emitter follower consisting of transistors 29 and 30 is to go high, then the voltage at the gate of transistor 33 will be low. This turns transistor 33 on to pull the output CKB all the way up to the supply voltage, V_d.

Thus there is provided a high speed, low cost, ECL to CMOS converter which can drive large capacitance loads found in many system applications.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the inventions.

What is claimed is:

1. Apparatus for converting low level input signals to CMOS level output signals, said apparatus comprising:

(a) a pre-amplifier coupled to receive said low level input signals,

(b) an output buffer operatively coupled to receive an output of said pre-amplifier, said output buffer having a first transistor in an emitter follower configuration, with the load of said emitter follower provided by a second transistor, and

(c) a circuit for generating a drive signal, said drive signal serving to turn off said second

transistor when the desired output of said emitter follower is a preselected logic level.

2. The apparatus of Claim 1 further comprising a third transistor, the input terminal of which is coupled to receive said drive signal, said third transistor connecting the output of said emitter follower to a preselected voltage when the desired output of said emitter follower is said preselected logic level.

3. The apparatus of Claim 1, further comprising a second buffer circuit operatively coupling the said one output of said pre-amplifier to said output buffer.

4. Apparatus for converting low level input signals to CMOS level signals, said apparatus comprising:

(a) a pre-amplifier coupled to receive said low level input signals and for producing two output signals, said two output signals being at opposite logic levels,

(b) first and second output buffers each operatively coupled to receive a different of said two output signals, each of said first and second output buffers having an emitter follower transistor, with the load of said emitter follower transistor provided by a second transistor, and

(c) a circuit for providing different drive signals for each of said second transistors, each said drive signal serving to turn off one of said second transistors when the desired output of the corresponding emitter follower is a preselected logic level.

5. The apparatus of Claim 4 further comprising a pair of third transistors, each of said pair of third transistors being associated with the emitter follower of one of said first and second output buffers and having an input terminal coupled to receive the drive signal for the second transistor of its associated emitter follower, said third transistor connecting the output of its

associated emitter follower to a preselected voltage when the desired output of the associated emitter follower is said preselected logic level.

6. The apparatus of Claim 4, further comprising intermediate buffer circuits, the first operatively coupling a first output of said pre-amplifier to said first output buffer and the second operatively coupling a second output of said pre-amplifier to said second output buffer.

7. A method for converting low level input signals to CMOS level output signals, said method comprising the steps of:

(a) applying said low level input signals to a pre-amplifier,

(b) operatively coupling a first output of said pre-amplifier to an output buffer, said output buffer having a first transistor in an emitter follower configuration, with the load of said emitter follower provided by a second transistor, and

(c) generating a drive signal, said drive signal serving to turn off said second transistor when the desired output of said emitter follower is a preselected logic level.

8. The method of Claim 7 comprising the further step of applying said drive signal to a third transistor, said third transistor connecting the output of said emitter follower to a preselected voltage when the desired output of said emitter follower is said preselected logic level.

9. The method of Claim 7 comprising the further step of applying said first output of said pre-amplifier to an intermediate buffer circuit and applying the output of said buffer circuit to said output buffer.

ABSTRACT

This invention relates to interfacing high speed, low voltage, data streams with CMOS circuits and, more specifically, to converting low voltage, differential, ECL signal levels to higher voltage levels which are compatible with CMOS circuits while maintaining high speed and sufficient drive capability for larger system applications. This is accomplished primarily by making the first stage inverters 5 and 6 as geometrically small as possible and providing additional cross-coupled buffers 7 and 8 capable of driving large capacitive loads.

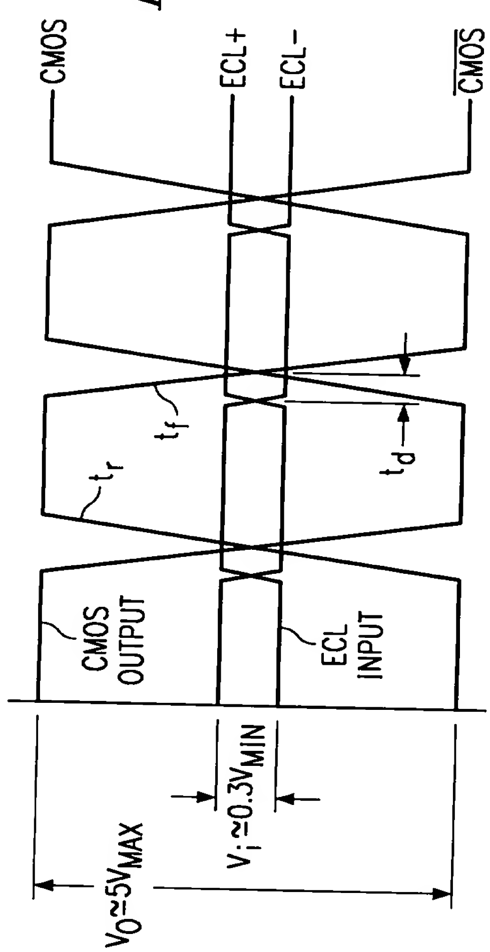
CMOS
ECL+
ECL-
$\overline{CMOS}$
CMOS OUTPUT
ECL INPUT
t_r
t_f
t_d
$V_O \simeq 5V_{MAX}$
$V_i \simeq 0.3V_{MIN}$

FIG. 1

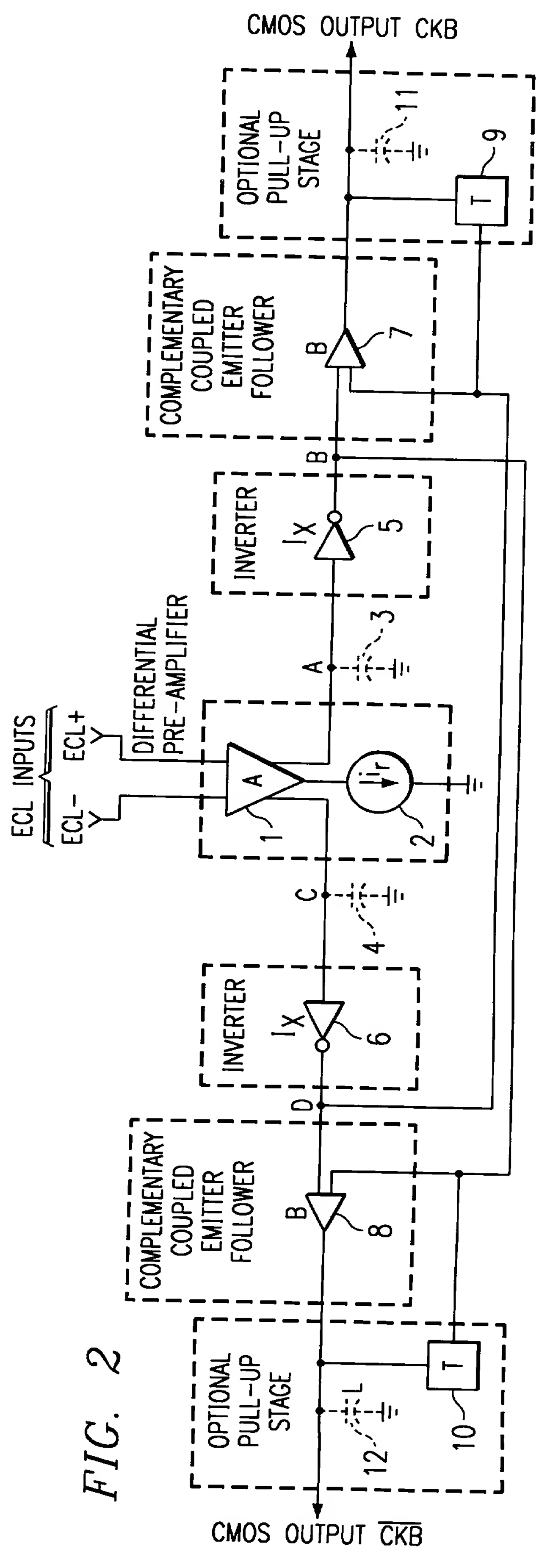
CMOS OUTPUT CKB
OPTIONAL PULL-UP STAGE
T
9
11
COMPLEMENTARY COUPLED EMITTER FOLLOWER
B
7
INVERTER
I_X
5
3
A
ECL INPUTS
ECL-
ECL+
DIFFERENTIAL PRE-AMPLIFIER
A
1
I_r
2
C
4
INVERTER
I_X
6
D
COMPLEMENTARY COUPLED EMITTER FOLLOWER
B
8
OPTIONAL PULL-UP STAGE
T
10
L
12
CMOS OUTPUT $\overline{CKB}$

FIG. 2

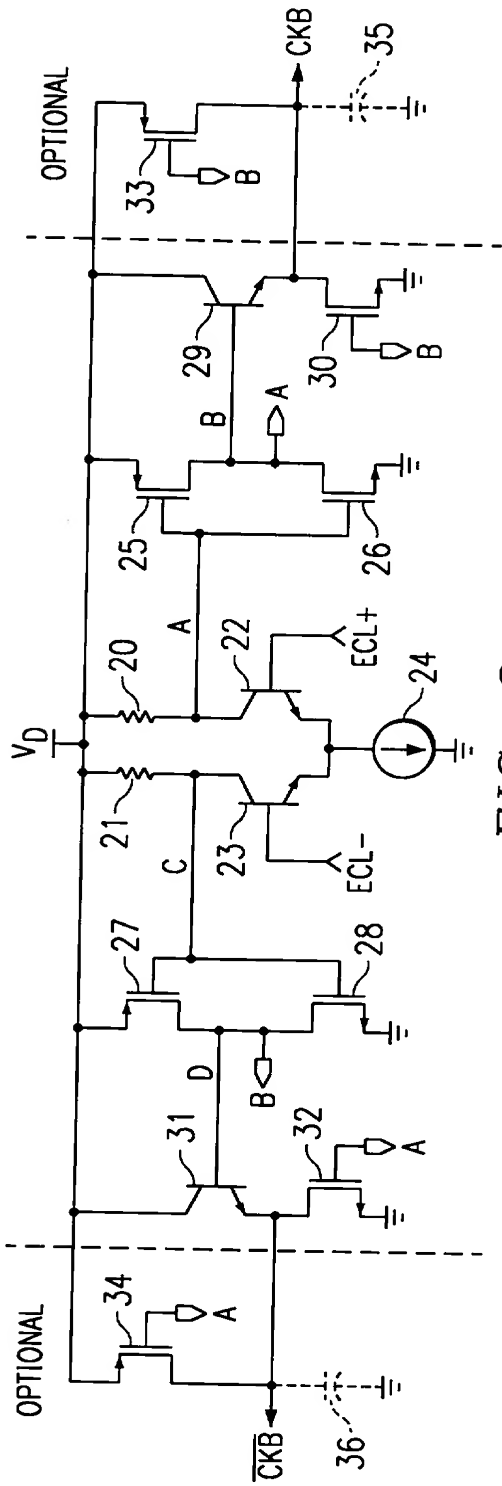
OPTIONAL
CKB
35
33
B
29
30
B
A
B
25
26
A
20
22
ECL+
24
V_D
21
C
23
ECL-
27
28
D
B
31
32
A
OPTIONAL
34
A
$\overline{CKB}$
36

FIG. 3

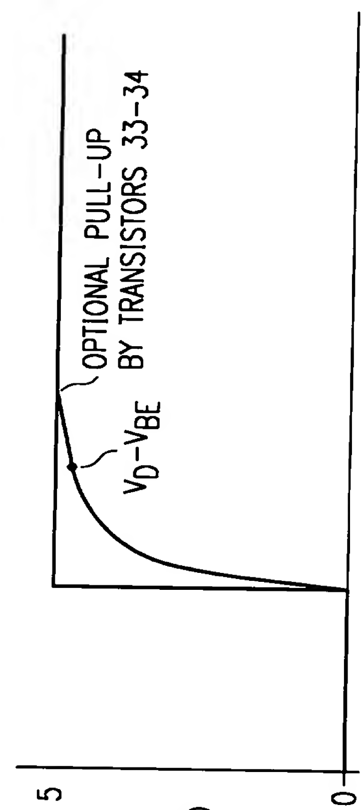
5
V_D
0
OPTIONAL PULL-UP
BY TRANSISTORS 33-34
V_D-V_{BE}

FIG. 4

RINT OF DRAWINGS
AS ORIGINALLY FILED

United States Patent & Trademark Office

Office of Initial Patent Examination -- Scanning Division

Application deficiencies found during scanning:

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